Listing of Claims:

1. (Original) A phase-locked loop circuit for providing an output signal having a frequency depending on the frequency of a reference signal, the circuit including means for deriving a feedback signal from the output signal, means for providing a control signal indicative of a phase difference between the reference signal and the feedback signal, means for controlling the frequency of the output signal according to the control signal, and means for causing the circuit to enter a lock condition when the reference signal and the feedback signal have the same frequency and a pre-defined phase difference means for causing the circuit to enter the lock condition includes means for conditioning the control signal to have an instantaneous value substantially zero in the lock condition by means of a conditioning signal consisting of a series of pulses each one corresponding to the pre-defined phase difference.

2. (Original) The circuit according to claim 1, wherein the means for providing the control signal includes means for generating a phase indicator signal consisting of a series of pulses each one indicative of a phase difference between the reference signal and the feedback signal, and wherein the means for conditioning includes means for adding the conditioning signal to the phase indicator signal, the pulses of the phase indicator signal being opposite to the pulses of the conditioning signal in the lock condition.

3. (Original) The circuit according to claim 2, wherein the means for generating the phase indicator signal includes means for setting a first indicator signal in response to a switching edge of the reference signal, means for setting a second indicator signal in response to the switching edge of the feedback signal, means for resetting the first indicator signal and the second indicator signal in response to the setting of both the first and the second indicator signals, and means for combining the first indicator signal and the second indicator signal into the phase indicator signal, the switching edges of the reference signal and of the feedback signal being synchronous with the pulses of the conditioning signal in the lock condition.

4. (Original) The circuit according to claim 1, wherein the means for conditioning includes means for generating the pulses of the conditioning signal

synchronously with a selected one between the reference signal and the feedback signal.

5. (Original) The circuit according to claim 4, wherein the selected signal consists of the feedback signal, the means for generating the conditioning signal including means for deriving the conditioning signal from the output signal.

6. (Original) The circuit according to claim 5, wherein the means for deriving the conditioning signal from the output signal includes means for generating the switching edge and a further switching edge of each pulse of the conditioning signal in response to a first switching edge and to a second switching edge, respectively, of the output signal, the second switching edge of the output signal corresponding to the switching edge of the feedback signal and the first switching edge of the output signal preceding the second switching edge of the output signal by a pre-defined number of periods of the output signal.

7. (Original) The circuit according to claim 6, wherein the means for generating the feedback signal includes a multi-modulus divider (for deriving a pre-scaled signal from the output signal, the means for deriving the conditioning signal from the output signal being clocked by the pre-scaled signal.

8. (Original) The circuit according to claim 1, wherein the phase-locked loop circuit is of a fractional type.

9. (Original) In a phase-locked loop circuit, a method of providing an output signal having a frequency depending on the frequency of a reference signal, the method including the steps of:

deriving a feedback signal from the output signal,

providing a control signal indicative of a phase difference between the reference signal and the feedback signal,

controlling the frequency of the output signal according to the control signal, and

causing the circuit to enter a lock condition when the reference signal and the feedback signal have the same frequency and a pre-defined phase difference,

wherein causing the circuit to enter the lock condition includes:

conditioning the control signal to have an instantaneous value substantially zero in the lock condition by means of a conditioning signal consisting of a series of pulses each one corresponding to the pre-defined phase difference.

10. (Original) A phase-locked loop for producing an output signal, comprising:

a first circuit operable to produce a first signal characterizing a phase difference between a feedback signal and a reference signal; and

a second circuit coupled to the first circuit, the second circuit operable to produce a second signal, the second circuit further operable to couple the second signal to the first signal to produce a control signal having an instantaneous value substantially equal to zero.

11. (Original) The loop of claim 10 wherein the control signal produces a locked condition of the loop.

12. (Original) The loop of claim 10 wherein the second signal has a rising edge corresponding to a rising edge of the feedback signal.

13. (Original) The loop of claim 10 wherein the second signal has a falling edge corresponding to a rising edge of the feedback signal.

14. (Original) The loop of claim 10 wherein the second circuit comprises a current source.

15. (Original) The loop of claim 14 wherein the second circuit further comprises a switch operable to transition between conducting and non-conducting states, the switch further operable to couple the current source to ground when in the conducting state.

16. (Original) The loop of claim 15 wherein the second circuit further comprises a third circuit operable to produce a third signal, the third signal operable to control the switch transitions.

17. (Original) The loop of claim 16 wherein the third circuit produces the third signal from the output signal.

18. (Original) The loop of claim 16, further comprising a fourth circuit operable to produce a fourth signal from the output signal, wherein the fourth signal clocks the third circuit.

19. (Original) A method of locking a phase-locked loop, comprising:

producing a first signal characterizing a phase difference between a feedback signal and a reference signal;

producing a second signal; and

producing a control signal comprising the first and second signals, the control signal having an instantaneous value substantially equal to zero.

20. (Original) An electronic system, comprising:

a phase-locked loop for producing an output signal, comprising:

a first circuit operable to produce a first signal characterizing a phase difference between a feedback signal and a reference signal; and

a second circuit coupled to the first circuit, the second circuit operable to produce a second signal, the second circuit further operable to couple the second signal to the first signal to produce a control signal having an instantaneous value substantially equal to zero.